VFTV010R013NA

Datasheet

General Description

The VFTV010R013NA is high voltage MOSFET utilizes charge balance technology to achieve outstanding low on-resistance and lower gate charge. It is engineered to minimize conduction loss, provide superior switching performance and robust avalanche capability. The VFTV010R013NA is optimized for extreme switching performance to minimize switching loss. It is tailored for high power density applications to meet the highest efficiency standards.

Symbol

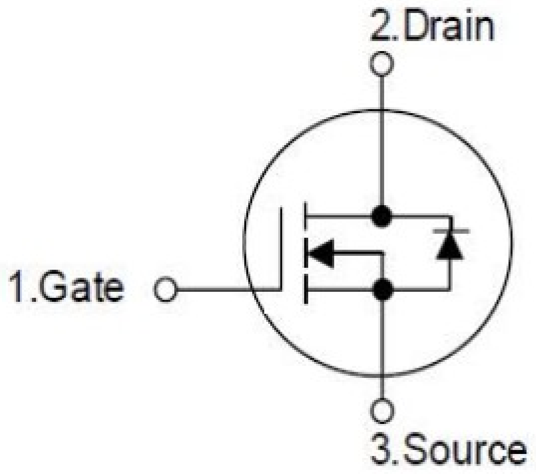


Figure 1 Symbol of VFTV010R013NA

Features

- $R_{DS(ON)\_max} = 1.3m\Omega@V_{GS} = 10V$
- Surface-mounted package
- Advanced trench cell design
- 100% UIS and Rg Tested

Package Type

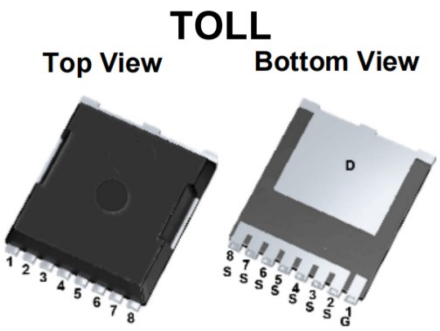


Figure 2 Package Type of VFTV010R013NA

Application

- Battery Management System
- Machine Tool
- High Power inverter system

Ordering Information

Product Name	Package
VFTV010R013NA	TOLL

Absolute Maximum Ratings (T_J= 25 ºC, unless otherwise specified)

Parameter		Symbol	Rating	Unit
Drain-Source Voltage		V_{DSS}	100	V
Gate-Source Voltage		V_{GSS}	±20	V
Continuous Drain Current Note 1	T_C=25ºC	I_D	395	A
	T_C=100ºC		250	
Pulsed Drain Current Tested	T_C=25ºC	I_{DM}	987	A
Continuous Diode Forward Current	T_C=25ºC	I_S	85	A
Max Power Dissipation	T_C=25ºC	P_D	313	W
	T_C=100ºC		125	
Continuous Drain Current Note 2	T_A=25ºC	I_D	40	A
	T_A=70ºC		32	
Max Power Dissipation Note2	T_A=25ºC	P_D	3.1	W
	T_A=70ºC		2	
Avalanche Current, Single pulse Note3	L=0.1mH	I_{AS}	100	A
	L=0.5mH		55	
Avalanche Energy, Single Pulse Note 3	L=0.1mH	E_{AS}	500	mJ
	L=0.5mH		152	
Max Junction temperature		T_J	150	ºC
Storage Temperature Range		T_{STG}	-55 to 150	

Thermal Resistance

Parameter	Symbol	Min	Typ	Max	Unit
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$		0.4		ºC/W
Thermal Resistance, Junction-to-Ambient Note2	$R_{\theta JA}$		40		

Notes:

1) Max. current is limited by max. junction temperature.
2) Surface Mounted on 1in^2 FR-4 board with 1oz
3) UIS tested and pulse width are limited by maximum junction temperature 150°C

Electrical Characteristics(T_J= 25 ºC, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Statistic Characteristics						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V, I_D=250uA	100			V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=80V, V_{GS}=0V			1	uA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V			±100	nA
Gate Threshold Voltage	$V_{GS(TH)}$	V_{DS}=V_{GS}, I_D=250uA	2.0		4.0	V
Static Drain-Source On-Resistance Note4	$R_{DS(ON)}$	V_{GS}=10V, I_D=30A		1.05	1.3	mΩ
Forward Transconductance	gfs	V_{DS}=5V, I_{DS}=50A		108		S
Gate Resistance	R_G	V_{GS}=0V, V_{DS}=0V Freq=1MHz		1.7		Ω
Dynamic Characteristics						
Input Capacitance	C_{ISS}	V_{DS}=50V V_{GS}=0V f=1MHz		13000		pF
Output Capacitance	C_{OSS}			2147		
Reverse Transfer Capacitance	C_{RSS}			398		
Turn-on Delay Time	$t_{d(on)}$	V_{DS}=50V I_{DS}=1A R_{GEN}=1Ω V_{GEN}=10V		27.7		ns
Turn-on Rise Time	t_r			21.5		
Turn-off Delay Time	$t_{d(off)}$			89.6		
Turn-off Fall Time	t_f			96.8		
Gate Charge Characteristics						
Gate to Source Charge	Q_{gs}	V_{GS}=10V V_{DS}=50V I_D=100A		70.2		nC
Gate to Drain Charge	Q_{gd}			65.7		
Gate Charge Total	Q_g			231		
Reverse Diode Characteristics						
Diode Forward Voltage Note5	V_{SD}	V_{GS}=0V, I_{SD}=30A		0.75	1.1	V
Reverse Recovery Time	t_{rr}	I_{DS}=30A,V_{GS}=0V di/dt=100A/us		120		ns
Reverse Recovery Charge	Q_{rr}			400		nC

4) Pulse test (pulse width<=300us, duty cycle<=2%)
5) Guaranteed by design, not subject to production testing.

Typical Performance Characteristics

Figure 3: Output Characteristics

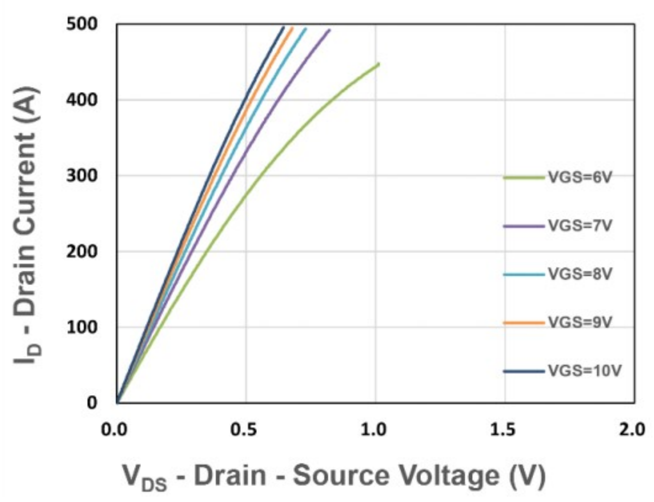


Figure 4: On-State Resistance vs ID

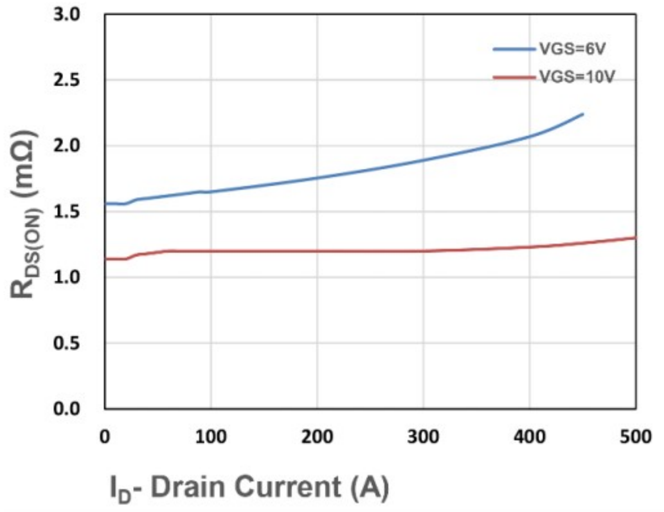


Figure 5: On-State Resistance vs VGS

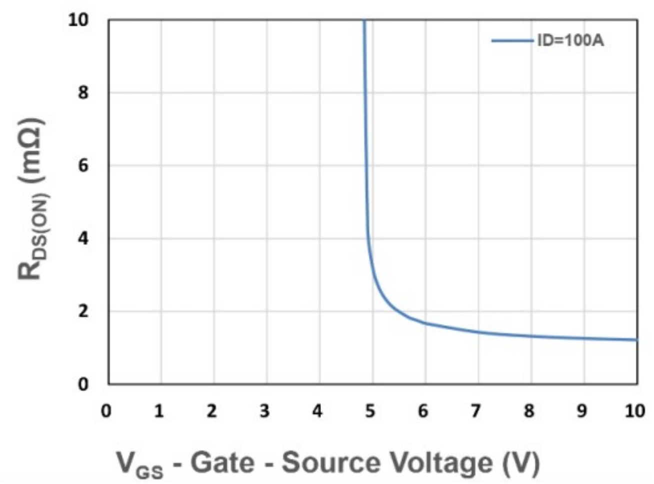


Figure 6: Gate Threshold Voltage

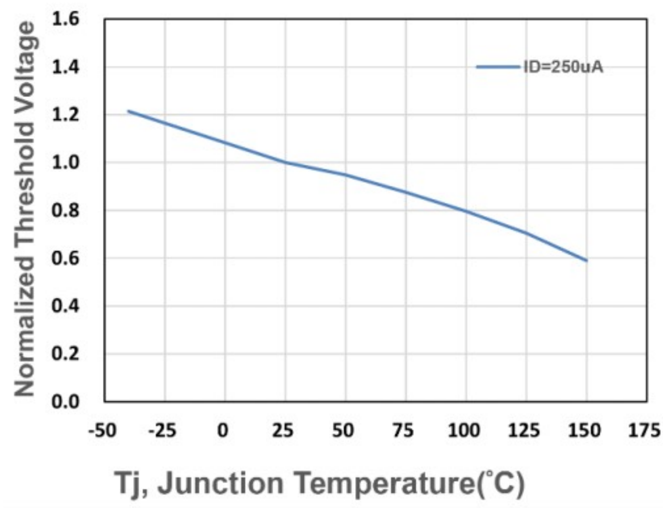


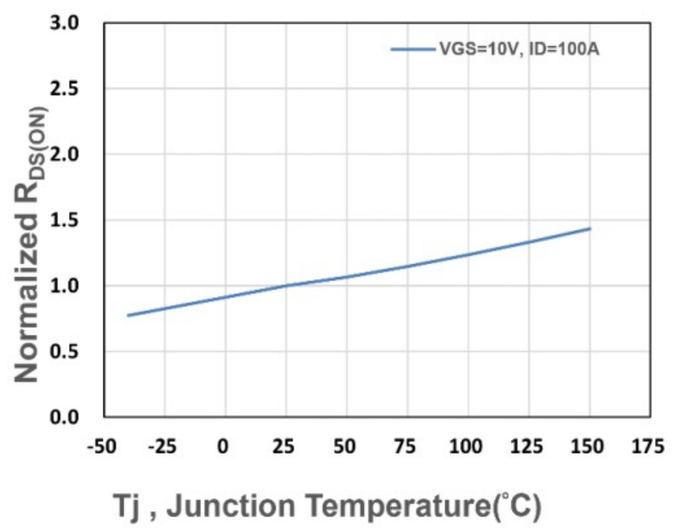
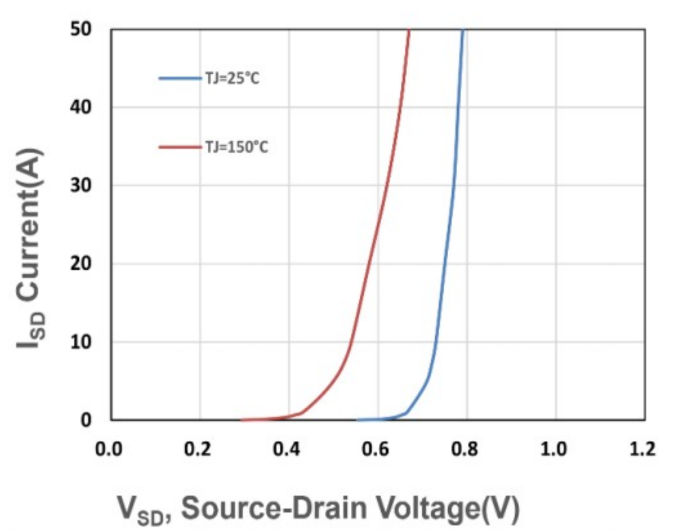
Figure 7: Drain-Source On-State Resistance	Figure 8: Source-Drain Diode Forward
	

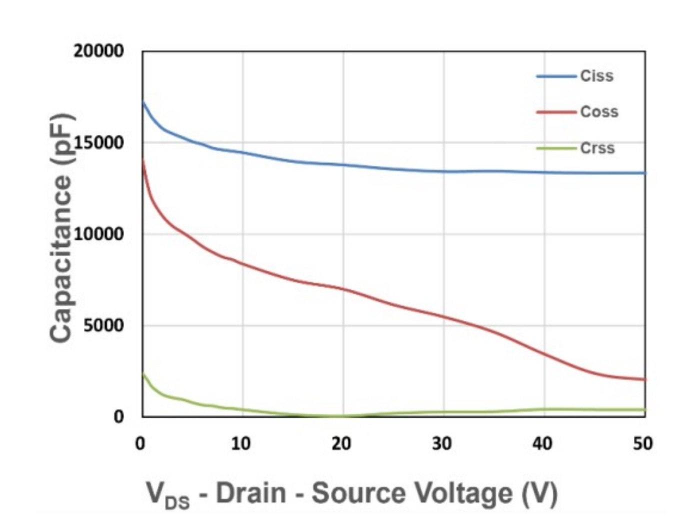
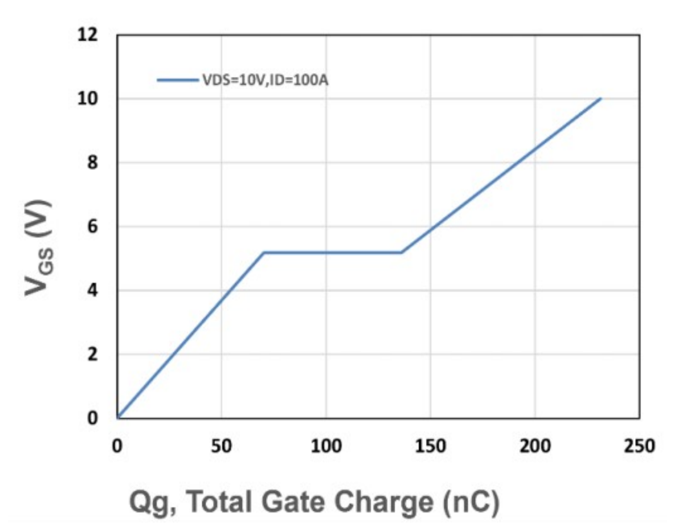
Figure 9: Typ. Capacitances	Figure 10: Gate Charge Characteristics
	

Figure 11: Power Dissipation	Figure 12: Drain Current

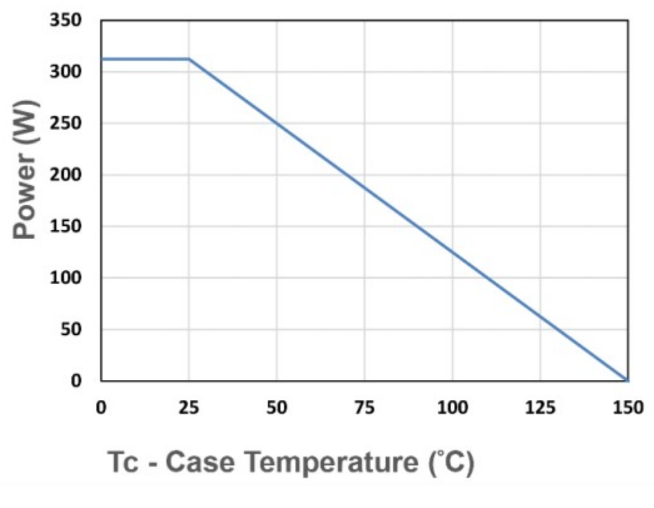
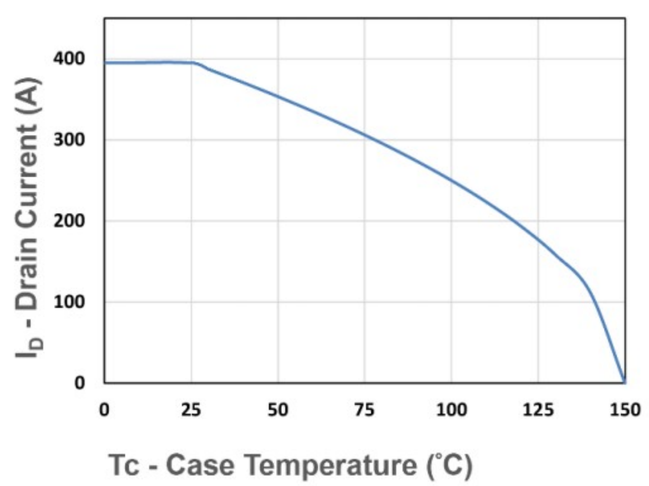

	

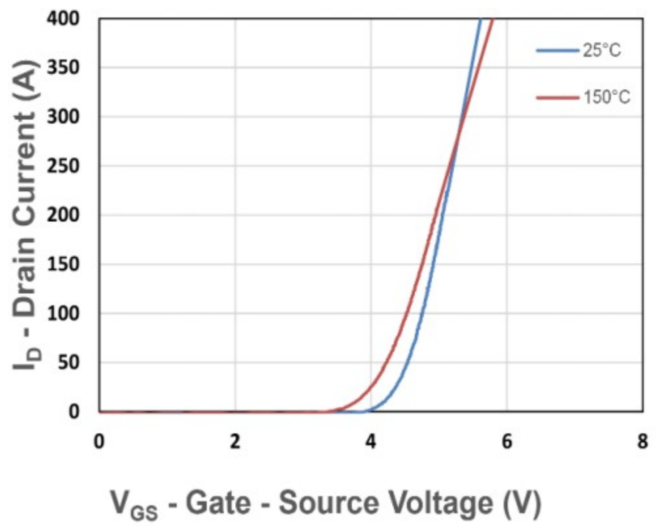
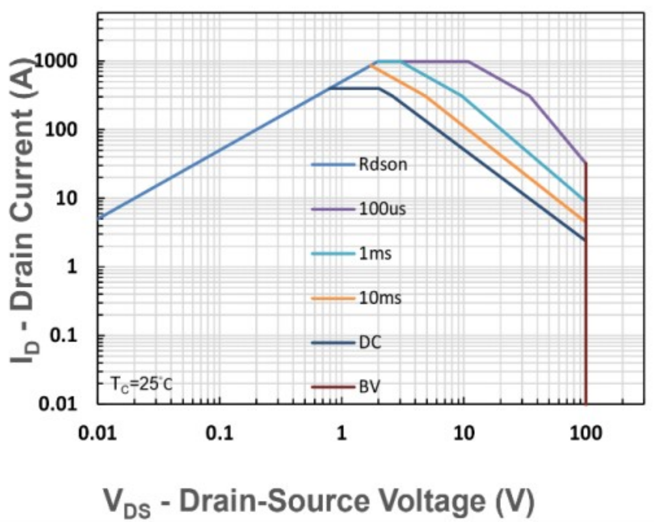
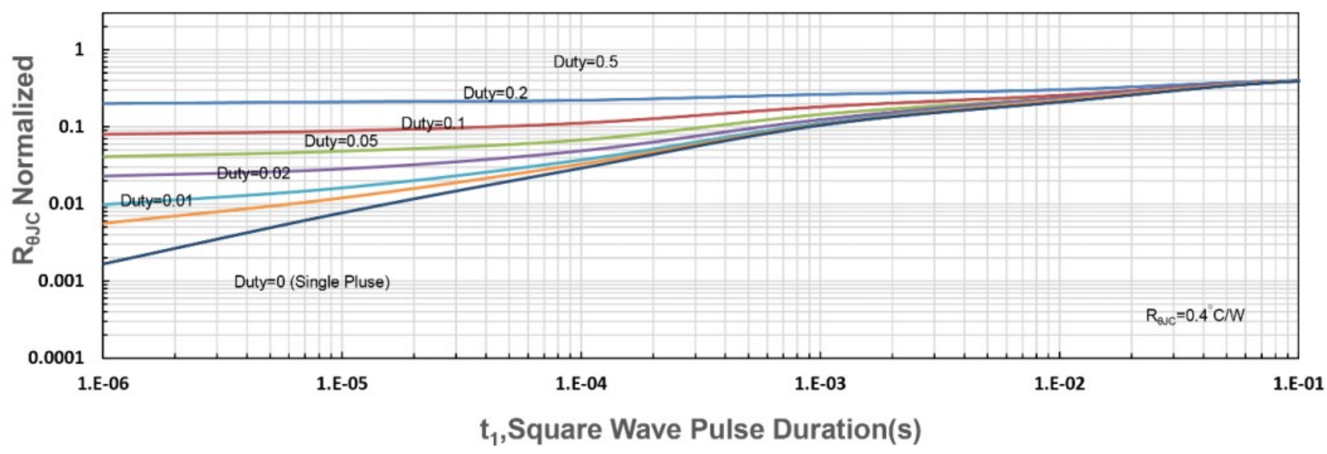
Figure 13: Transfer Characteristics	Figure 14: Safe Operating Area
	

Figure 15: $R_{\theta JC}$ Transient Thermal Impedance



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